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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/430,366 10/28/99 RAMSBEY

M M-7523-US

EXAMINER

MMC2/0717

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ART UNIT

PAPER NUMBER

2813

DATE MAILED:

07/17/00

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

# Office Action Summary

Application No.  
09/430,366

Applicant(s)  
Ramsbey et al.

Examiner  
Jack Chen

Group Art Unit  
2813



☒ Responsive to communication(s) filed on May 12, 2000

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

## Disposition of Claims

☒ Claim(s) 1-20 is/are pending in the application.

Of the above, claim(s) 16-20 is/are withdrawn from consideration.

☐ Claim(s) \_\_\_\_\_ is/are allowed.

☒ Claim(s) 1-15 is/are rejected.

☐ Claim(s) \_\_\_\_\_ is/are objected to.

☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.

## Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on \_\_\_\_\_ is ☐ approved ☐ disapproved.

☒ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some\* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) \_\_\_\_\_.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\*Certified copies not received: \_\_\_\_\_

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). \_\_\_\_\_

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

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### DETAILED ACTION

1. Claims 16-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 3.

### *Specification*

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 1, the term “substantially” is unclear.

Re claim 2, the term “high quality” is indefinite.

Re claim 7, lines 4-5, the term “the floating gate” lacks antecedent basis.

Re claim 7, the term “substantially” is unclear.

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Re claim 8, the term "high quality" is indefinite.

Re claim 13, the term "the floating gate" lacks antecedent basis.

Re claim 13, the term "the vertical surfaces" lacks antecedent basis.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

6. Claims 1, 2, 4-8, 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamauchi et al., U.S./5,962,889.

Yamauchi et al. discloses a method for forming a semiconductor device, which comprises providing a substrate 1; forming tunnel oxide 2 on the substrate; depositing a floating gate layer on the tunnel oxide, the floating gate layer having a first thickness; etching the floating gate layer to form floating gate 3; depositing an insulator 7 on the substrate, the insulator covering the floating gate, a portion of the insulator not covering the floating gate having a second thickness that is greater than the first thickness; and polishing the insulator until the second thickness is

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substantially equal to the first thickness, whereby polishing the insulator produces a floating gate and insulator layer, see figs. 1A-14E, cols. 1-14.

7. Claims 1, 2, 4-8, 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Chan et al., U.S./6,051,467.

Chan et al. discloses a method for forming a semiconductor device, which comprises providing a substrate 10; forming tunnel oxide 16 on the substrate; depositing a floating gate layer 18 on the tunnel oxide, the floating gate layer having a first thickness; etching the floating gate layer to form floating gate 18; depositing an insulator 30 on the substrate, the insulator covering the floating gate, a portion of the insulator not covering the floating gate having a second thickness that is greater than the first thickness; and polishing the insulator until the second thickness is substantially equal to the first thickness (fig. 5), whereby polishing the insulator produces a floating gate and insulator layer, figs. 11, cols. 1-8.

8. Claims 1, 2, 5, 7, 8, 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu, U.S./6,033,956.

Wu discloses a method for forming a semiconductor device, which comprises providing a substrate 200; forming tunnel oxide 202 on the substrate; depositing a floating gate layer on the tunnel oxide, the floating gate layer having a first thickness; etching the floating gate layer to form floating gate 204; depositing an insulator 210 on the substrate, the insulator covering the floating gate, a portion of the insulator not covering the floating gate having a second thickness that is greater than the first thickness; and polishing/planarizing the insulator until the second thickness is

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substantially equal to the first thickness, whereby polishing the insulator produces a floating gate and insulator layer, see figs. 1-4G, cols. 1-6.

9. Claims 1, 2, 4-8, 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamagishi et al., U.S./5,808,339.

Yamagishi et al. discloses a method for forming a semiconductor device, which comprises providing a substrate 11; forming tunnel oxide 51 on the substrate; depositing a floating gate layer on the tunnel oxide, the floating gate layer having a first thickness; etching the floating gate layer to form floating gate 52/53; depositing an insulator 54 on the substrate, the insulator covering the floating gate, a portion of the insulator not covering the floating gate having a second thickness that is greater than the first thickness; and polishing the insulator until the second thickness is substantially equal to the first thickness, whereby polishing the insulator produces a floating gate and insulator layer, see figs. 1-12B, cols. 1-16.

### ***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 3, 9, 13, 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi et al., U.S./5,962,889 or Chan et al., U.S./6,051,467 or Wu, U.S./6,033,956 or

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Yamagishi et al., U.S./5,808,339 taken with Ogura et al., U.S./5,672,892 or Hong, U.S./5,478,767 in view of Applicant's admitted prior art.

However, the above references do not explicitly show using doped polysilicon or doped amorphous silicon for the floating gate, and thermally oxidizing the floating gate to seal the vertical surfaces of the floating gate.

It is well known in the art to use doped polysilicon or doped amorphous silicon for the floating gate, such will increase the conductivity of the floating gate. For example, Applicant's admitted prior art teaches using doped polysilicon or doped amorphous silicon for the floating gate, see pages 1-2. It is also well known in the art to thermally oxidizing the floating gate to seal the vertical surfaces of the floating gate such will provide isolation (eliminate short circuit) from the adjacent gates or device elements, and keep charges within the floating gate. For example, Ogura et al. teaches thermally oxidizing the floating gate to seal the vertical surfaces of the floating gate, see figs. 1-5, cols. 1-16; Hong also teaches thermally oxidizing the floating gate to seal the vertical surfaces of the floating gate, see figs. 1-4K, cols. 1-10.

With respect to claims 3 and 9, the thickness of the layers are considered to involve routine optimization which has been held to be within the level of ordinary skill in art. Although the above references do not fall into the ranges of the inventor's disclosure, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to vary the thickness of the layers for optimization purposes. More particularly, where the general conditions

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of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.

Furthermore, the implanting energy, dosage, thickness, width are considered to involve routine optimization which has been held to be within the level of ordinary skill in the art. As noted in *In re Aller*, the selection of reaction parameters such as energy, dosage, thickness, width and temperature, etc. would have been obvious:

“Normally, it is to be expected that a change in energy, concentration, thickness, dosage, temperature, or combination of any of them would be an unpatentable modification.

Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed “critical ranges and the applicant has the burden of proving such criticality....

More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.”

*In re Aller* 105 USPQ233, 255 (CCPA 1955). See also *In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmischer* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sola* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any energy, concentration, thickness, width range suitable to the method in



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process of Yamauchi et al., U.S./5,962,889 or Chan et al., U.S./6,051,467 or Wu, U.S./6,033,956 or Yamagishi et al., U.S./5,808,339 in order to optimize the process.

Furthermore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the standard process of Yamauchi et al. or Chan et al. or Wu or Yamagishi et al. with the teaching of (Ogura et al. or Hong) and Applicant's admitted prior art because of the desirability to improve device reliability and performance of the device.

### ***Conclusion***

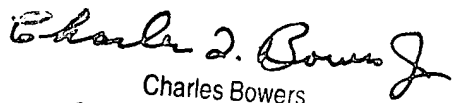
12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (703) 308-5838. The examiner can normally be reached on Monday-Friday from 8:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers, can be reached on (703) 308-2417.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jack Chen

July 13, 2000

  
Charles Bowers  
Supervisor Patent Examiner  
Technology Center 2800